MICROCOMPUTER BASED [redacted]ECTRONIC TRIP SYSTEM FOR CI[redacted]IT BREAKERS.

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- european:
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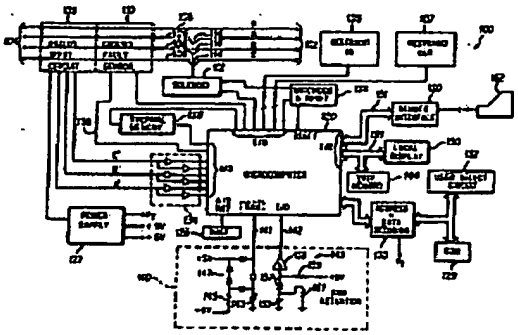
IE903136 (A1)
EP0440764 (A4)
EP0440764 (B1)
more >>

Cited documents:
WO8805973
FR1558647
EP0193447
US4209818

Abstract not available for EP0440764
Abstract of correspondent: **US5136458**

A processor-based tripping system uses a precise three phase current detection circuit using a minimal number of components. A set of current sensors is situated adjacent the current path to sense respective phases of current therein. The current sensors provide respective current signals therefrom which are fed to a ground fault transformer. The ground fault transformer includes input inductors connected to respective ones of the current sensors such that current flowing through each respective current sensor also flows through one of the input inductors. An output inductor in the ground fault transformer is coupled with the input inductors for adding the current signals from the current sensors and for producing an output current signal in the presence of a ground fault. The output current signal is then rectified to provide a rectified signal corresponding to the output current. The processor receives the rectified signal to detect the ground fault in the three phase current path and provides a trip signal to a solenoid to break the current path. The ground fault transformer also includes a test input inductor for receiving an external AC signal to simulate a ground fault.



Data supplied from the ***esp@cenet*** database - Worldwide

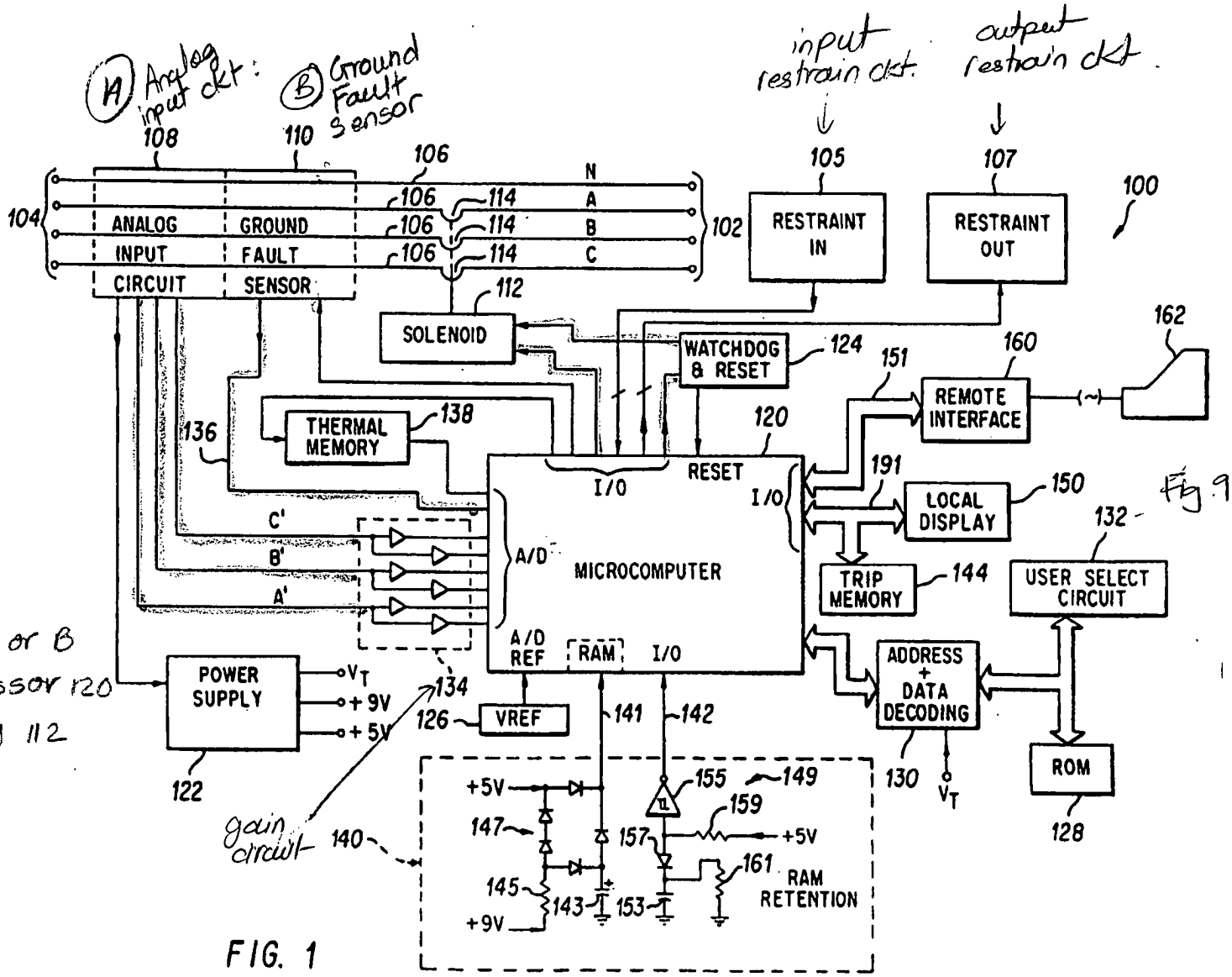


FIG. 1

Fig 9

Inputs from A or B to microprocessor 120 can trip solenoid 112

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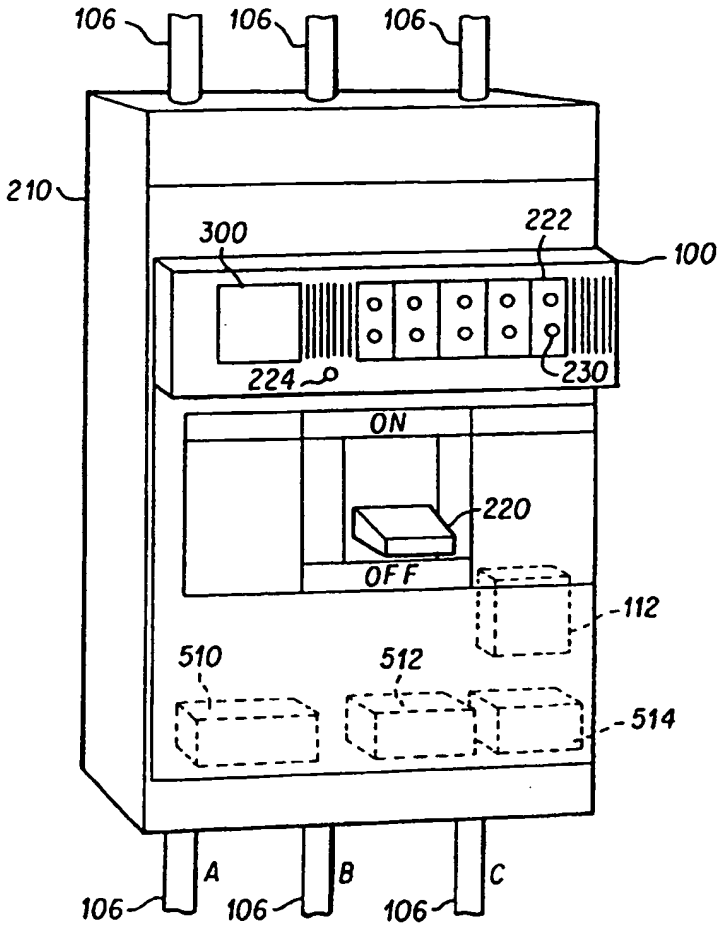
106
106
106
210
300
222
100
224
230
ON
220
OFF
112
510
512
514
A
B
C
106
106
106

FIG. 2

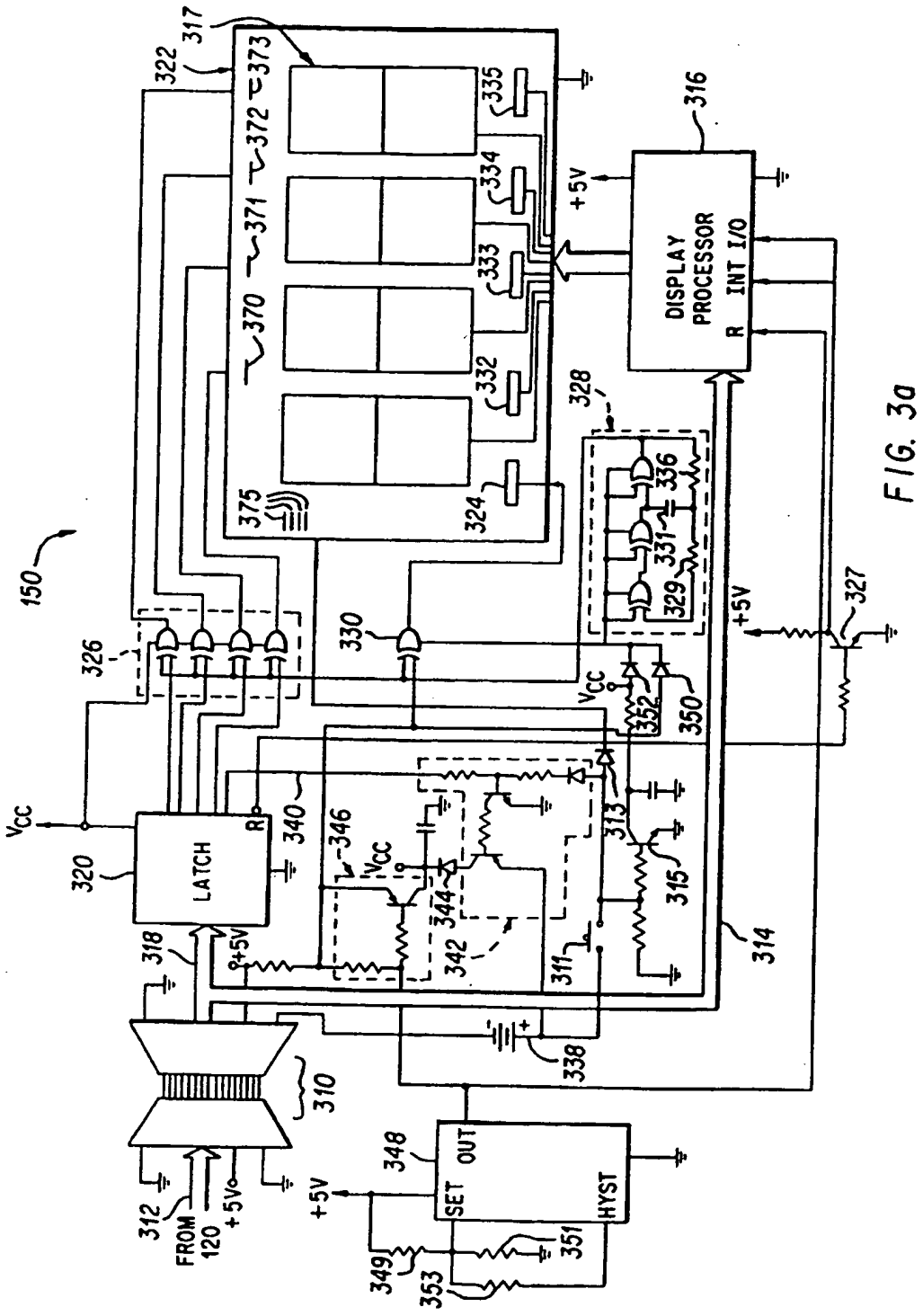
150
317
322
373
372
371
370
375
335
334
333
332
324
316
+5V
DISPLAY PROCESSOR
R INT I/O
328
336
331
329
327
326
330
Vcc
352
350
340
346
313
315
320
LATCH
R
318
+5V
342
344
311
314
338
310
348
SET
OUT
HYST
351
349
353
312
FROM 120
+5V

FIG. 3a

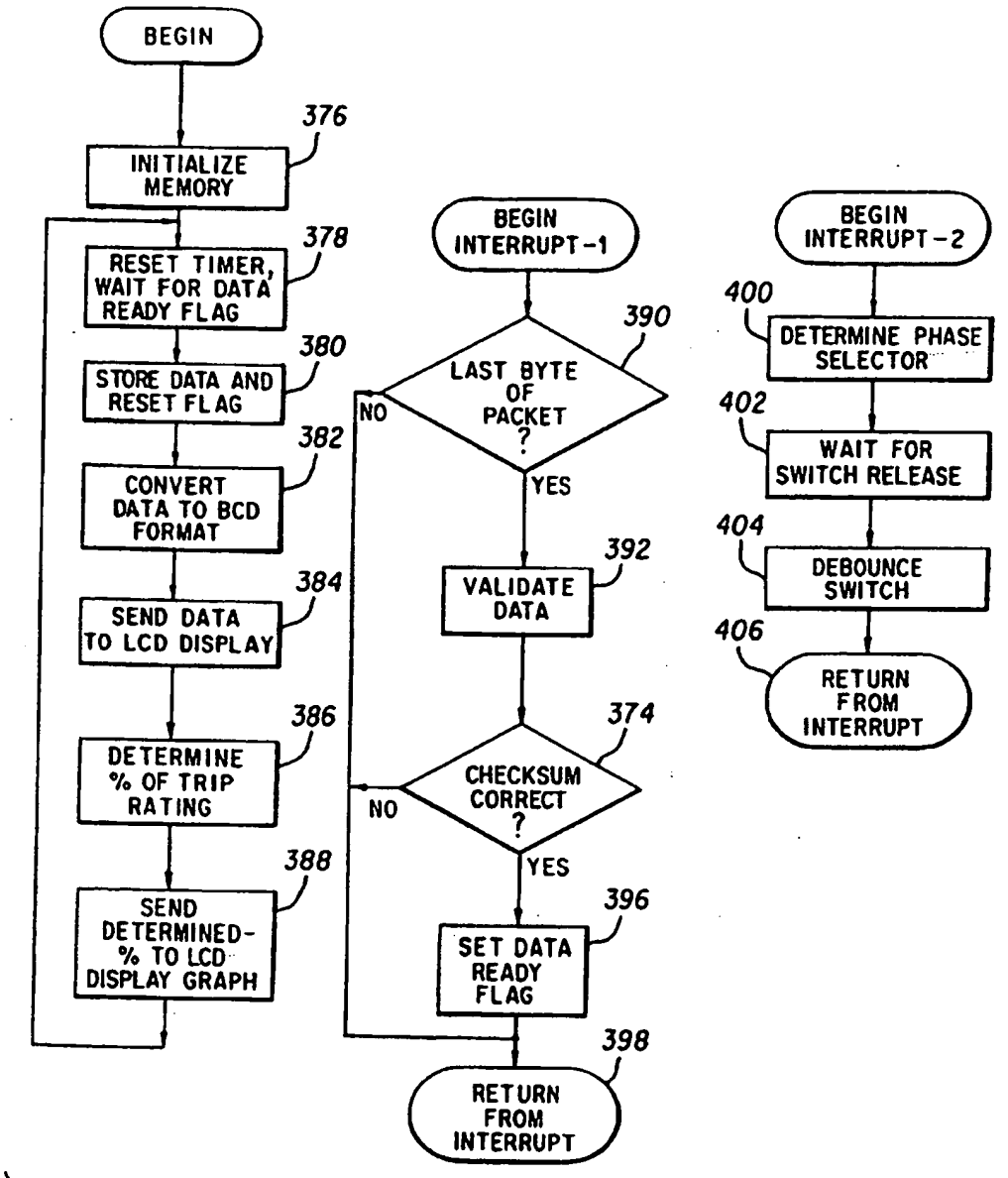
BEGIN
376
INITIALIZE MEMORY
378
RESET TIMER, WAIT FOR DATA READY FLAG
380
STORE DATA AND RESET FLAG
382
CONVERT DATA TO BCD FORMAT
384
SEND DATA TO LCD DISPLAY
386
DETERMINE % OF TRIP RATING
388
SEND DETERMINED-% TO LCD DISPLAY GRAPH
BEGIN INTERRUPT-1
390
LAST BYTE OF PACKET ?
NO
YES
392
VALIDATE DATA
374
CHECKSUM CORRECT ?
NO
YES
396
SET DATA READY FLAG
398
RETURN FROM INTERRUPT
BEGIN INTERRUPT-2
400
DETERMINE PHASE SELECTOR
402
WAIT FOR SWITCH RELEASE
404
DEBOUNCE SWITCH
406
RETURN FROM INTERRUPT

FIG. 3b

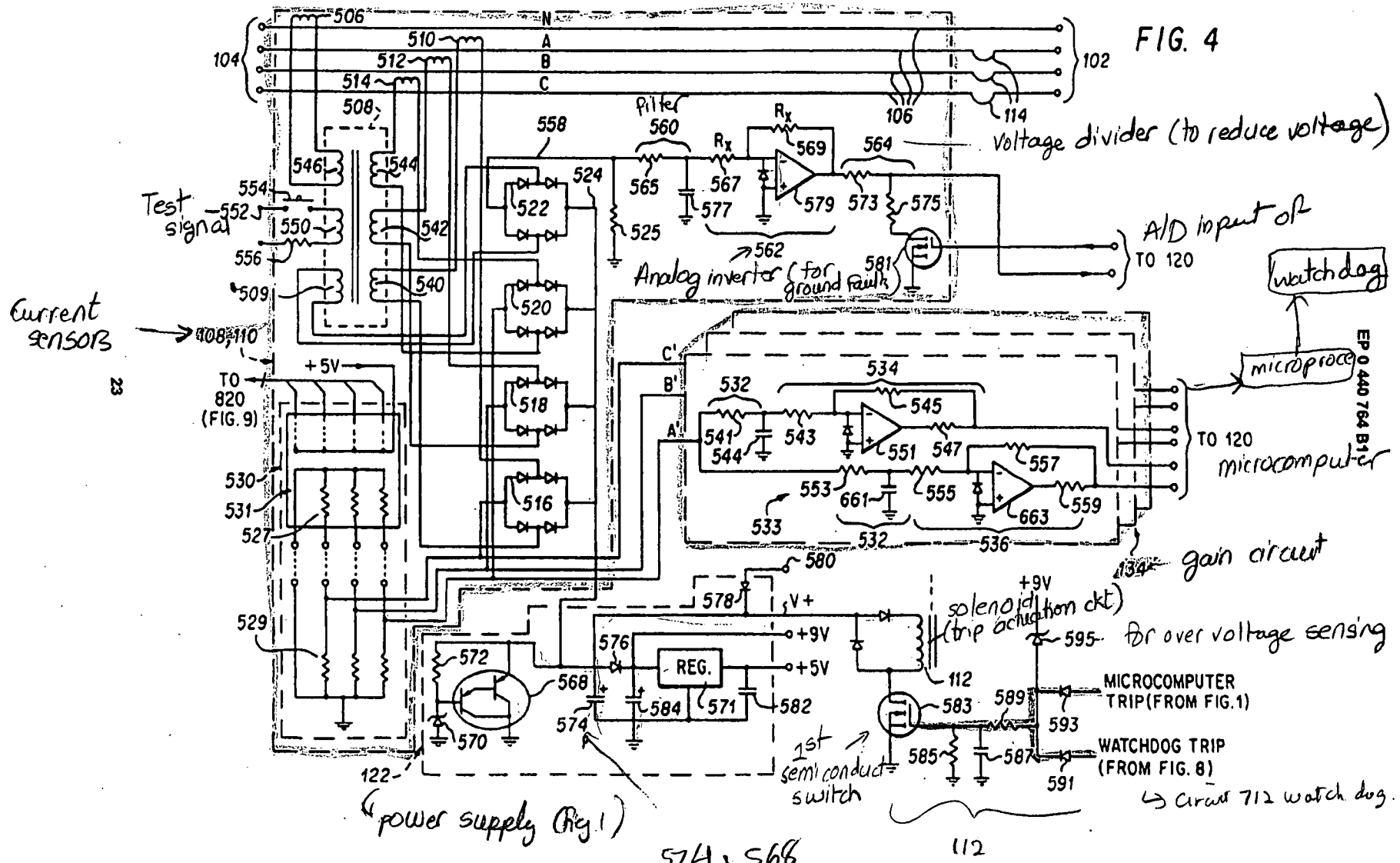
FIG. 4
Current sensors
Test signal
Voltage divider (to reduce voltage)
A/D input of
TO 120
Analog inverter (for ground fault)
watchdog
microproce
TO 120
microcomputer
gain circuit
solenoid (trip actuation ckt)
for over voltage sensing
MICROCOMPUTER TRIP(FROM FIG.1)
WATCHDOG TRIP (FROM FIG. 8)
circuit 712 watch dog.
1st semiconduct switch
power supply (Fig.1)
574 & 568
112
see page 9,22-27
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23

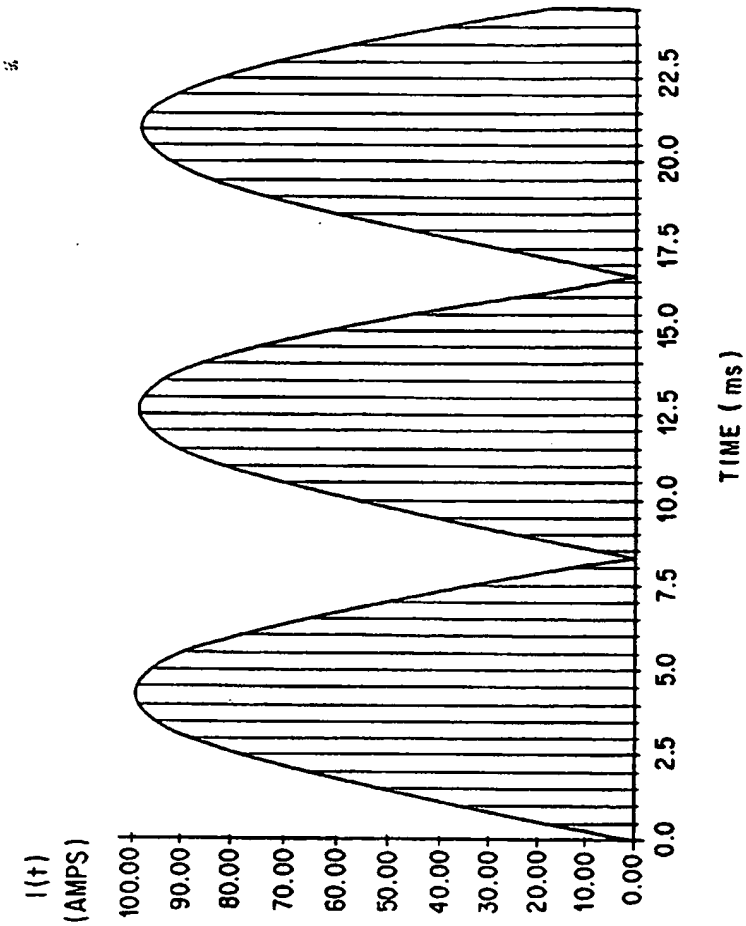
I(t)
(AMPS)
100.00
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
0.0
2.5
5.0
7.5
10.0
12.5
15.0
17.5
20.0
22.5
TIME (ms)

FIG. 5

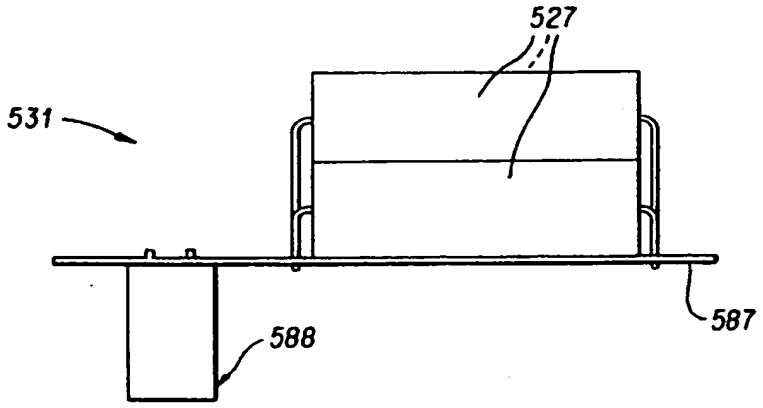

FIG. 6a

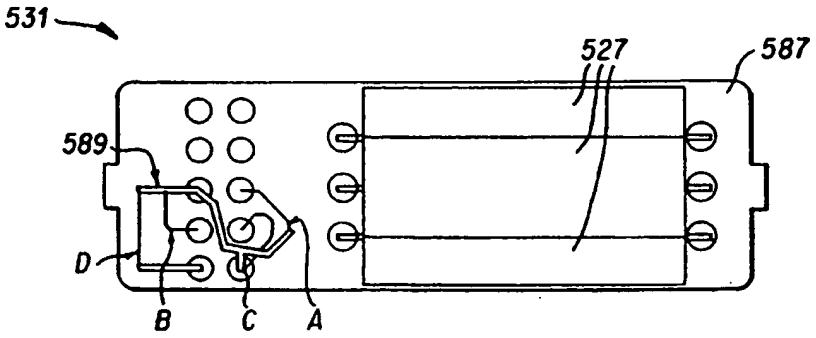

FIG. 6b

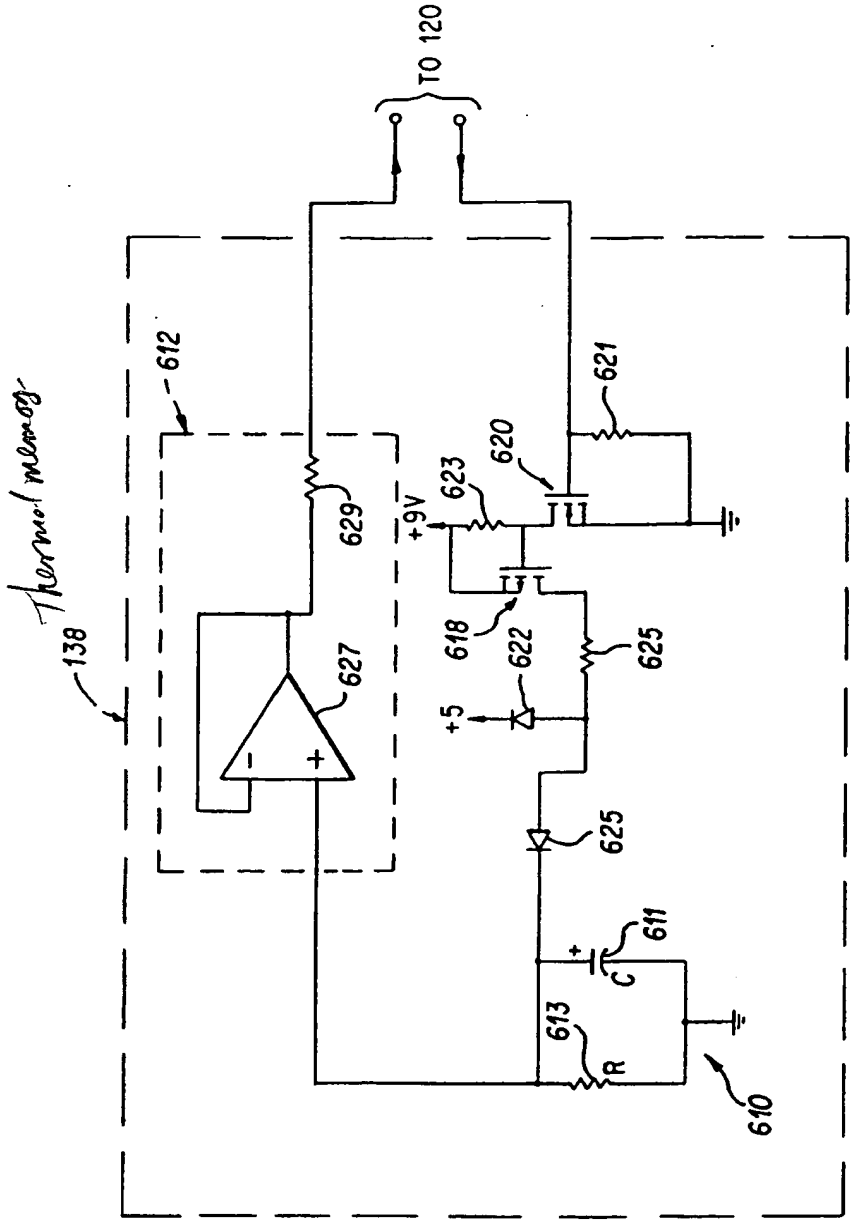
TO 120
612
621
620
623
+9V
629
618
622
625
627
+5
138
625
611
C
613
R
610

FIG. 7

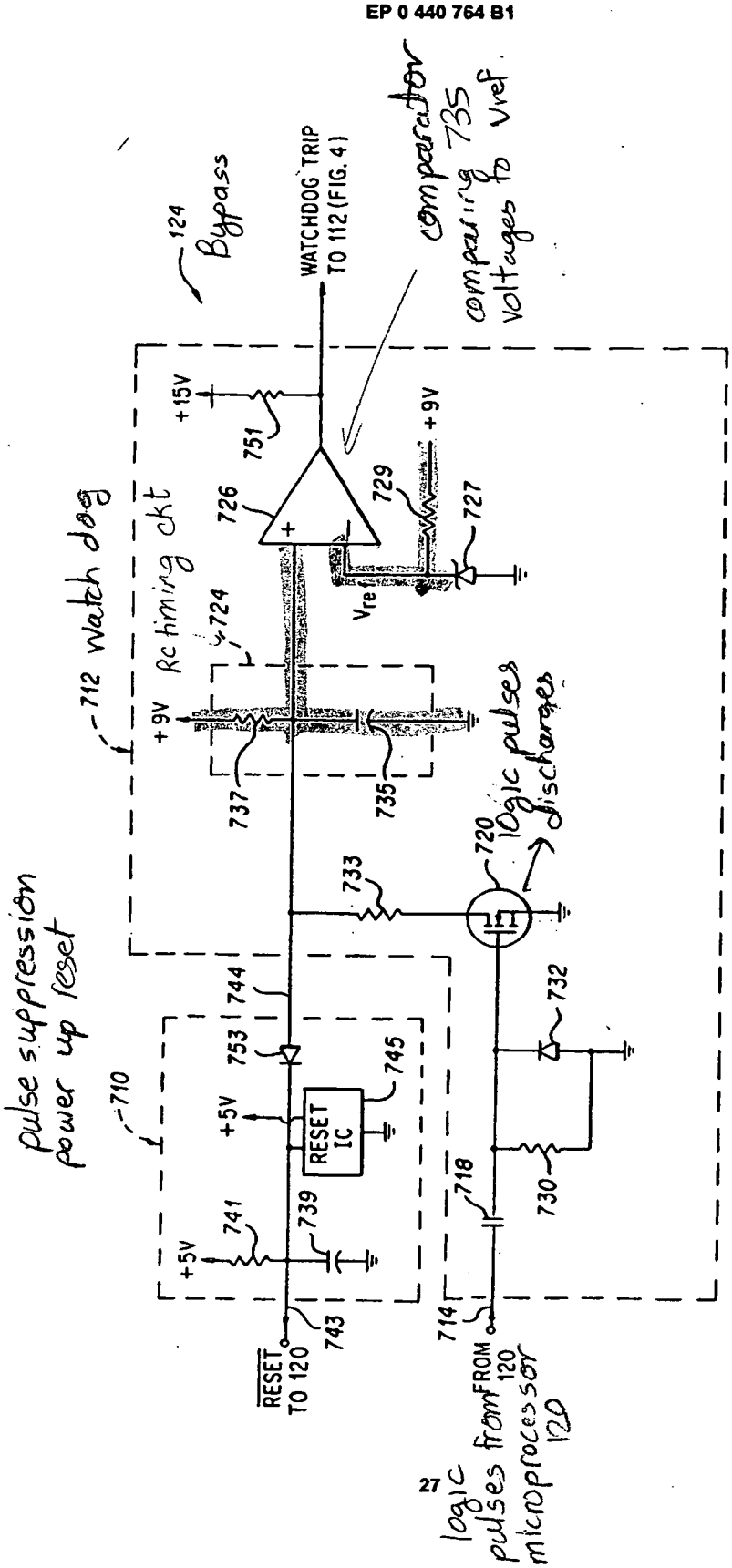
124
Bypass
WATCHDOG TRIP
TO 112 (FIG. 4)
comparator
comparing 735
voltages to Vref.
712 watch dog
RC timing ckt
724
+15V
751
+9V
729
727
726
V_{ref}
+9V
737
735
720
logic pulses
discharges
733
732
744
753
745
+5V
RESET
IC
710
pulse suppression
power up reset
741
739
+5V
718
730
743
714
RESET
TO 120
FROM
120
logic
pulses from
microprocessor
120
27

FIG. 8 (page 12)

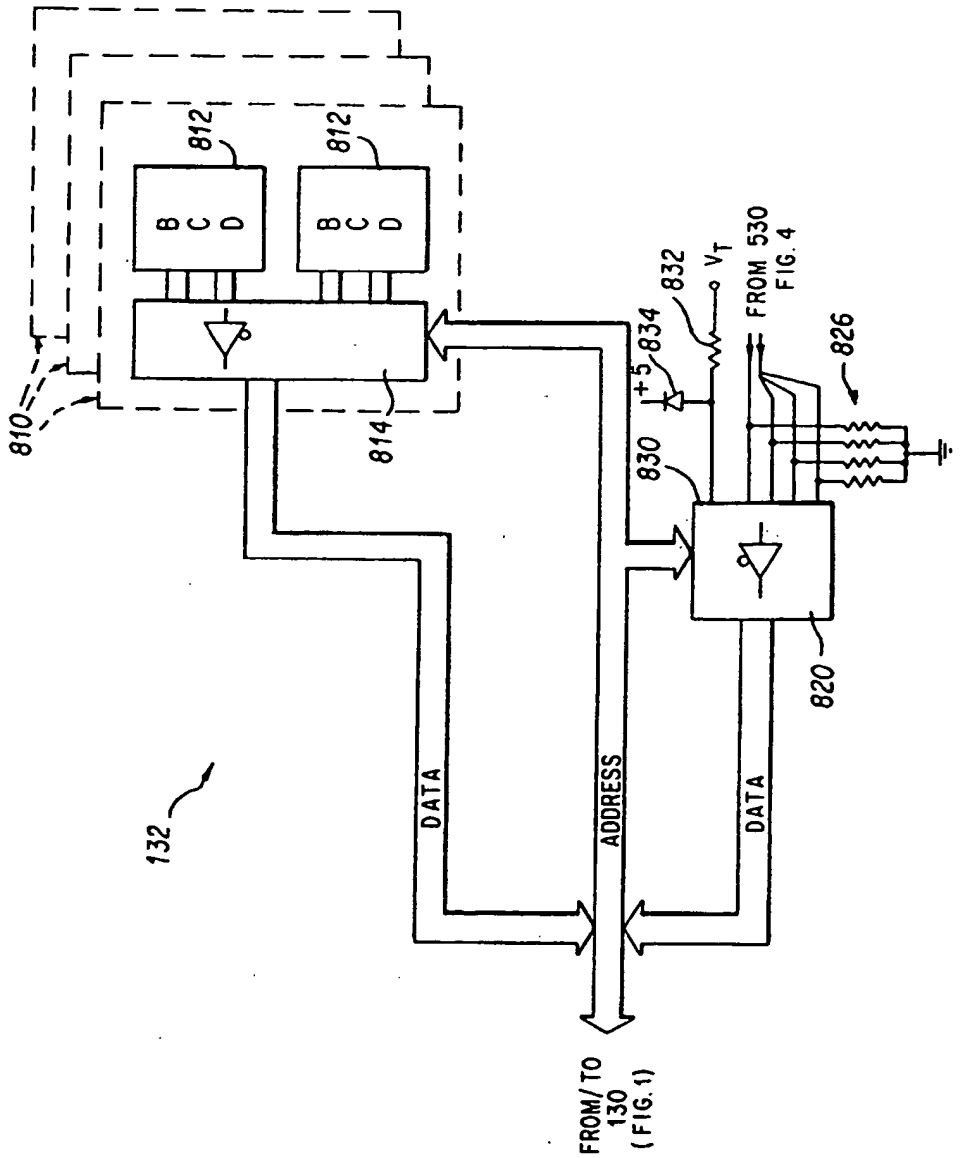
810
812
812
B C D
B C D
814
832
V_T
834
+5
FROM 530 FIG. 4
826
830
820
132
DATA
ADDRESS
DATA
FROM/TO 130 (FIG. 1)

FIG. 9